REMARKS/ARGUMENTS

In the Office Action mailed January 14, 2008, claims 1-7 were rejected. Additionally, claims 1, 5, 6, and 7 were objected for minor informalities. In response, Applicants hereby request reconsideration of the application in view of the amendments and the below-provided remarks. No claims are added or canceled.

For reference, claims 1-7 are amended. In particular, claims 1-7 were amended to fix the minor grammatical informalities. Specifically, claims 1, 6, and 7 were amended to remove the word "characterised." Additionally, claim 1 was amended to clarify reference to a circuit to connect a storage capacitor Cst of a selected gate line GLy to the additional gate off supply line VLclean. Additionally, claim 2 was amended for clarification of PMOS and NMOS transistors, MP1, MN1, and MN2 in association with the additional supply line VLclean. Additionally, claims 4 and 5 were amended to clarify associations between the supply line VL and the additional supply line VLclean. Additionally, claim 5 was amended to remove an improper use of parenthesis. Additionally, claims 6 and 7 were amended to fix the layout and punctuation of the claims. Additionally, claims 6 and 7 were amended to properly reference previous and next gate lines being activated, respectively. Additionally, claims 6 and 7 were amended to clarify reference to the supply line VL, the additional supply line VLclean, and the separate track of the additional supply line VLclean. The amendments of claims 1-7 are supported, for example, by the subject matter described in the specification on page 5, lines 17-25, page 11, line 29 to page 12, line 8, the abstract, Fig. 10, and Fig. 11b.

Claim Rejections under 35 U.S.C. 102

Claims 1-7 were rejected under 35 U.S.C. 102(b) as being anticipated by Eu (U.S. Pat. Pub. No. 2002/0080133, hereinafter Eu). However, Applicants respectfully submit that these claims are patentable over Eu for the reasons provided below.

Independent Claims 1, 6 and 7

Claim 1 recites "an additional gate off supply line VLclean to substantially reduce a discharge time associated with driving transistors of the LC-Display, wherein the additional gate off supply line is coupled to the output stages of the gate drivers and is routed as a separate track from the gate off supply line VL," and "a circuit to connect a storage capacitance Cst reference terminal of a selected gate line GLy to the additional gate off supply line VLclean and to keep other storage capacitors Cst of unselected gate lines connected to the gate off supply line VL" (emphasis added). Claims 6 and 7 recite similar limitations.

In contrast, Eu does not disclose an additional low supply line, VClean, to substantially reduce a discharge time associated with driving transistors of the LC-Display that is routed as a separate track from the low supply line VL. Eu merely discloses using a discharge circuit attached to a gate driver IC. Eu, paragraphs 24, 25, and 33; Figs. 2 and 4. In particular, Eu discloses a gate high voltage Vgh 20, a gate low voltage Vgl 22, and an additional voltage supply line 24. Eu, paragraphs 33-34. Although Eu discloses an additional voltage supply line 24, the additional voltage supply line 24 is different from the additional low supply line VClean because the voltage supply line 24 does not an act as an additional gate low voltage Vgl 22. The additional voltage supply line 24 does not connect to the gate driver IC 14 like the Vgh 20 and Vgl 22 lines. The Vgl 22 line works in connection with the PMOS transistor M2 in the gate driver IC 14 to turn off an active transistor on a liquid crystal display of Eu. With regard to the voltage line 24, Eu is concerned with controlling a PNP-type transistor Q1 and a NPN-type transistor Q2 to form a short between the first input line 20 and the second input line 22.

Furthermore, even if the voltage supply line 24 was understood to disclose an additional gate off supply line, in general, Eu nevertheless fails to disclose an additional gate off supply line that is routed as a separate track from the . In fact, Eu appears to be silent with regard to routing an additional low supply line as a separate track on the LC-display glass. Therefore, Eu does not disclose an additional low supply line VLclean routed as a separate track from the low supply line VL because Eu merely discloses a priority-based flow control mechanism.

Moreover, Eu does not disclose a circuit to connect a storage capacitance Cst of a selected gate line GLy to the additional gate off supply line VLclean and to keep other storage capacitors Cst of unselected gate lines connected to the gate off supply line VL. In fact, it appears that Eu is silent with regard to a circuit to connect a storage capacitance Cst of a selected gate line GLy to the additional gate off supply line VLclean and to keep other storage capacitors Cst of unselected gate lines connected to the gate off supply line VL.

For the reasons presented above, Eu does not disclose all of the limitations of the claim because Eu does not disclose an additional low supply line VClean to substantially reduce a discharge time associated with driving transistors of the LC-Display that is routed as a separate track on the LCD glass, as recited in the claim. Neither does Eu disclose a circuit to connect a storage capacitance Cst reference terminal of a selected gate line GLy to the additional gate off supply line VLclean and to keep other storage capacitors Cst of unselected gate lines connected to the gate off supply line VL. Accordingly, Applicants respectfully assert claims 1, 6 and 7 are not anticipated by Eu because Eu does not disclose all of the limitations of the claims.

Dependent Claims

Claims 2-5 depend from and incorporate all of the limitations of the corresponding independent claim 1. Applicants respectfully assert claims 2-5 are allowable based on allowable base claims. Additionally, each of claims 2-5 may be allowable for further reasons, as described below.

Claim 2 recites "a PMOS transistor MP1 arranged between the supply line VH and the output of the output stage, a first NMOS transistor MN1 arranged between the supply line VL and the output of the output stage, and a second NMOS transistor MN2 arranged between the additional supply line VLclean and the output of the output stage" (emphasis added). In contrast, the cited portion of Eu (paragraphs 24, 25, and 33; Figs. 2 and 4) merely discloses an NMOS transistor M1 connected between the high input line Vgh 20 and the gate line GL, and a PMOS transistor M2 connected between the low input line Vgl 22 and the gate line GL. As shown in Fig. 4, and described in paragraphs 30-35, Eu only discloses a single NMOS transistor M1 and a single PMOS transistor M2

for a given gate line GL. In fact, Eu appears to be silent with regard to a second NMOS transistor that is connected between an additional supply line and the output of the output stage, or gate line GL. Therefore, Eu does not disclose all of the limitations of claim 2 because Eu does not disclose a second NMOS transistor MN2 arranged between the additional supply line VLclean and the output of the output stage, as recited in the claim. Accordingly, Applicants respectfully assert claim 2 is not anticipated by Eu because Eu does not disclose all of the limitations of the claim.

Claim 3, as amended, recites "the additional gate off supply line VLclean is routed over a separate track on the LC-Display glass" (emphasis added). In contrast, the cited portion of Eu generally refers to a discharge circuit, a gate driver IC, and a data driver IC. Eu, Fig. 2. In fact, it appears that Eu is silent with regard to routing a separate track on the LC-Display glass. Therefore, Eu does not disclose all of the limitations of claim 3 because Eu does not disclose the additional gate off supply line VLclean is routed over a separate track on the LC-Display glass, as recited in the claim. Accordingly, Applicants respectfully assert claim 3 is not anticipated by Eu because Eu does not disclose all of the limitations of the claim.

Claim 4, as amended, recites "a track of the low supply line VL and a track of the additional supply line VLclean are coupled to a same supply level" (emphasis added). In contrast, the cited portion of Eu generally refers to a discharge circuit, a gate driver IC, and a data driver IC. Eu, paragraphs 28 and 31, Figs. 2 and 4. Specifically, Eu discloses that at startup the voltage level of first input line 20 is set at +18V to +25V, the voltage level of the second input line 22 is set at -5V to -8V, and the voltage level of the third input line 24 is set at +7V to +10V. Eu, paragraph 33. Thus, the additional supply line 24 could not possibly be coupled to the same supply level as the first input line 20 or the second input line 22 since all three input lines of Eu are set to different voltage levels relative to one another at startup. Therefore, Eu does not disclose all of the limitations of claim 4 because Eu does not disclose a track of the low supply line VL and a track of the additional supply line VLclean are coupled to a same supply level, as recited in the claim. Accordingly, Applicants respectfully assert claim 4 is not anticipated by Eu because Eu does not disclose all of the limitations of the claim.

Claim 5, as amended, recites "a track of the low supply line VL and a track of the additional supply line VLclean are connected together in a location where a track impedance to an output of the power supply is relatively low" (emphasis added). In contrast, the cited portion of Eu generally refers to a discharge circuit, a gate driver IC, and a data driver IC. Eu, paragraphs 28 and 31, Figs. 2 and 4. As described above, Eu discloses that the first, second, and third input lines 20, 22, and 24 are connected to different voltage supply levels. Eu, paragraph 33. Thus, the additional supply line 24 could not possibly be connected together with either the first input line 20 or the second input line 22, nor could the first input line 20 be connected together to the second input line 22 since any two lines connected together would share the same voltage level. Since all three input lines of Eu are set to different voltage levels relative to one another at startup, none of the input lines of Eu are connected together. Therefore, none of the input lines of Eu could be connected together in a location where a track impedance to an output of the power supply is relatively low. Thus, Eu does not disclose all of the limitations of claim 5 because Eu does not disclose a track of the low supply line VL and a track of the additional supply line VLclean are connected together in a location where a track impedance to an output of the power supply is relatively low, as recited in the claim. Accordingly, Applicants respectfully assert claim 5 is not anticipated by Eu because Eu does not disclose all of the limitations of the claim.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3444** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3444** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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